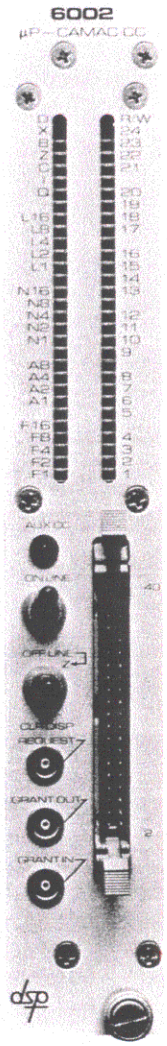
DSP TECHNOLOGY
MODEL 6001 & 6002, PC001 & PC004

Microcomputer Crate Controller & Dataway Display

FEATURES:

- IBM PC/XT/AT and Apple II interfaces available. Generally compatible with microcomputer type busses.
- High Speed Data transfer (to 700 Kbytes per second on IBM PC).
- Built-in Dataway Display simplifies system maintenance and program development.
- Use personal computers to read and control sophisticated CAMAC equipment very economically.
- Set up an intelligent test/readout/display station at each point in a multi-disciplinary lab.
- Excellent for educational laboratory or training in data acquisition and control systems.
- Data Acquisition and Control Software available for IBM PC/XT/AT.



APPLICATIONS:

Over 600 plug-in modules in the international CAMAC Standard (IEEE Std. #583 and ESONE Report 4100e) are available from more than 30 companies for data acquisition and process control. These modules are powered by a standard 19" rack-mounted CAMAC crate and are completely interchangeable and compatible. The crate contains a parallel data bus of 24 bits each for reading and writing. A standard protocol exists for the interface of each module to the Dataway.

The computer interface is located in the rightmost two slots of the CAMAC crate. DSP Technology Corporation has developed a module that allows data collection, process (experiment) control and display by today's most-popular computers.

The DSP Technology Model 6001 is a combined CAMAC Crate Controller and Dataway Display Module, packaged in a 2-width module. This saves one CAMAC slot normally necessary for the display function, a very useful tool in debugging data acquisition software.

The module accepts data and commands from the microprocessor, executes the CAMAC commands and provides data back to the microprocessor. Direct memory access (DMA) data transfers are implemented for the IBM PC/XT/AT microcomputer. The status of the last CAMAC cycle executed is displayed on the front panel LEDs.

The DSP Technology Model 6002 is a Type 2 CAMAC Crate Controller which permits use in a position other than the rightmost station of the crate as an auxiliary crate controller (ACC). This allows access to the data in the modules from a host computer as well as from the secondary controller (For example, Apple, S 100, or IBM). This module can also function as a standard Crate Controller.

AVAILABLE MICROCOMPUTER INTERFACES

PC001: APPLE II PLUS Interface card, cable, and a 5¼" diskette with a CAMAC software driver running under Applesoft Basic are provided.

PC004: IBM PC Interface card, cable and software driver for programmed I/O and DMA transfers (up to 700 Kbytes per second). Software drivers for Microsoft Basic, Fortran, Pascal and Borland Turbo Pascal (source code written in Assembly is also provided). Controls up to four Camac crates. User installed jumpers for LAM interrupt servicing.

TECHNICAL SPECIFICATIONS

Model 6001 & 6002, PC001 & PC004 Microcomputer Crate Controller & Dataway Display

FRONT PANEL CONTROL/DISPLAY

LED Indicators: Display the result of the last CAMAC command executed. LAM lights, which are priority encoded, are on whenever a module generates a LAM.

Clear Display: Push button which clears the display.

Clear Dataway: Generates a CAMAC clear.

I/O: 40 pin connector which interfaces the module to the host computer.

6002 Only: 3 LEMO connectors for Grant In/Grant Out/Requests LED indicates ACC/CC operation offline/online switch.

PACKAGING

CAMAC #2 Module (IEEE Std #583 and ESONE Report 4100e).

POWER REQUIREMENTS

+6V: 1.3A.

CAMAC RESPONSES & COMMANDS

LAMs: The CAMAC LAMs (Look at Me) are priority encoded with station 1 as highest priority and 23 as lowest.

A flag bit is generated on signal that LAM is on.

Q, X: The Q and X bits reflect the status of the CAMAC X and Q lines during the last CAMAC cycle.

Z, C: A CAMAC Initialize or Clear command may be generated by loading the appropriate bit of register A6 and initiating a CAMAC cycle. These bits are reset after the CAMAC cycle is completed.

I: Sets the CAMAC inhibit line.

AUXILIARY CONTROL BUS

6002 includes CAMAC standard auxiliary control bus-see IEEE Std #583.

Data read or written is passed over a byte-wide, bidirectional bus controlled by four address lines and six control lines. The four address lines which select internal registers for reading/writing data are:

Address	Address Lines				Function
	BA8	BA4	BA2	BA1	
A0	L	L	L	L	Stores CAMAC WH BYTE (W17-W24) Data
A1	L	L	L	H	Stores CAMAC WM BYTE (W9-W16) Data
A2	L	L	H	L	Stores CAMAC WL BYTE (W1-W8) Data
A3	L	L	H	H	Stores CAMAC A Subaddress Data (0-15)
A4	L	H	L	L	Stores CAMAC F Function Data (0-31)
A5	L	H	L	H	Stores CAMAC N Station Data (0-23)
A6	L	H	H	L	Stores CAMAC Z,C,I, and Aux Inhibit Hold Control Data
A7	L	H	H	H	Starts a CAMAC cycle
A8	H	L	L	L	Reads CAMAC Q,X, and encoded LAM
A9	H	L	L	H	Reads RH BYTE (R17-R24) Data
A10	H	L	H	L	Reads RM BYTE (R9-R16) Data
A11	H	L	H	H	Reads RL BYTE (R1-R8) Data
A12	H	H	L	L	Reads Status Register (LSB-CAMAC Cycle Complete, LSB+1-ACL State, LSB+2-High for on line)

The six control lines are:

BDS: Master enable which must be low to address the unit.

BR/W: Controls data flow on the bidirectional bus-high to read, low when addressing registers 0-6 and high for registers 8-11.

BQ3: Timing signal used when writing data into the unit.

CC: Active low TTL pulse initiates CAMAC Cycle.

L: Active low TTL when LAM is present.

Q: Q status of last CAMAC cycle.